APPLICATION FOR

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SPECIFICATION

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Title of the Invention: LOGICAL CIRCUIT DESIGNING DEVICE, LOGICAL CIRCUIT DESIGNING METHOD, STORAGE MEDIUM AND PROGRAM

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Background of the Invention

Field of the Invention

The present invention relates to a linkage technology between a logical circuit designing tool and a transmission line circuit analysis tool and, in particular a logical circuit designing device, a logical circuit designing method, a storage medium and a program for feeding back a logical circuit modified using a transmission line circuit analysis tool to a logical design tool.

Description of the Related Art

Lately, a variety of digital technologies, such as the design technology and production technology of LSIs, have remarkably advanced. For example, very high-performance CPUs have been integrated in one chip. The storage capacity of a semi-conductor memory has also remarkably increased. Thus, digital technologies have rapidly advanced in a variety of aspects.

For example, a variety of software technologies, such as the software technology of man-machine interface, have also advanced.

Thanks to the progress of such digital and software technologies, for example, a CAD apparatus using a computer, such as EWS (engineering workstation), has been used in a design field, such as an electrical circuit designing and the like.

In a conventional logical circuit design, a logical circuit is first generated using a tool for making logical circuits, a transmission line circuit is further generated by manual input work based on the logical circuit in order to verify this logical circuit.

Although the transmission line circuit used to verify the logical circuit is modified to reflect the verification result, this modification result must also be reflected on the logical circuit by manual input work.

However, when a transmission line circuit is generated from a logical circuit generated using a tool for making logical circuits, in most cases, only both output and input can be distinguished and the transmission line circuit must be edited by an editor. For that reason, the generation of the transmission line circuit requires much labor and the reliability is reduced.

Summary of the Invention

The present invention is made in view of the

problem, and it is an object of the present invention to provide a logical circuit designing device, a logical circuit designing method, a storage medium and a program for automating work manually done and implementing both the reduction of labor and the improvement of data reliability.

The logical circuit designing device of the present invention comprises a logical circuit storage unit, a transmission line circuit generation unit, a transmission line circuit storage unit, a transmission line circuit editing unit and a logical circuit modification unit.

In the first aspect of the present invention, the logical circuit storage unit stores a logical circuit. The transmission line circuit generation unit generates a transmission line circuit based on the logical circuit stored in the logical circuit storage unit. The transmission line circuit storage unit stores the transmission line circuit generated by the transmission line circuit generation unit.

In the second aspect of the present invention, the logical circuit storage unit stores a logical circuit. The transmission line circuit storage unit stores a transmission line circuit corresponding to the logical circuit stored in the logical circuit storage unit. The

transmission line circuit editing unit edits the transmission line circuit stored in the transmission line circuit storage unit. The logical circuit modification unit modifies the corresponding logical circuit based on the transmission line circuit edited by the transmission line circuit editing unit.

In the third aspect of the present invention, the logical circuit storage unit stores a logical circuit. The transmission line circuit generation unit generates a transmission line circuit based on the logical circuit stored in the logical circuit storage unit. The transmission line circuit storage unit stores the transmission line circuit generated by the transmission line circuit generation unit. The transmission line circuit editing unit edits the transmission line circuit stored in the transmission line circuit storage unit. The logical circuit modification unit modifies the corresponding logical circuit based on the transmission line circuit edited by the transmission line circuit editing unit.

Brief Description of the Drawings

Fig. 1 shows the overall configuration of a logical circuit designing device adopting the present invention;

Fig. 2 shows the principle of a logical circuit designing device adopting the present invention;

Fig. 3 shows the overall configuration of the first preferred embodiment of the present invention;

Fig. 4 shows an example of topology designation (general);

Fig. 5 shows an example of topology designation (star type);

Fig. 6 shows an example of topology designation (single-stroke brushing type);

Fig. 7 shows an example of the value designation of a resistor, a capacitor or a coil (logical circuit);

Fig. 8 shows an example of the value designation of a resistor, a capacitor or a coil (value designation table);

Fig. 9 shows an example of the value designation of a resistor, a capacitor or a coil (transmission line circuit);

Fig. 10 shows an example of the addition designation of a resistor, a capacitor or a coil (logical circuit);

Fig. 11 shows an example of the addition designation of a resistor, a capacitor or a coil (addition designation table);

Fig. 12 shows an example of the addition

designation of a resistor, a capacitor or a coil (transmission line circuit);

Fig. 13 shows an example of the deletion designation of a resistor, a capacitor or a coil (logical circuit);

Fig. 14 shows an example of the deletion designation of a resistor, a capacitor or a coil (addition designation table);

Fig. 15 shows an example of the deletion designation of a resistor, a capacitor or a coil (transmission line circuit);

Fig. 16 shows an example of the value modification of a resistor, a capacitor or a coil (logical circuit: original);

Fig. 17 shows an example of the value modification of a resistor, a capacitor or a coil (transmission line circuit);

Fig. 18 shows an example of the value modification of a resistor, a capacitor or a coil (logical circuit: after modification);

Fig. 19 shows an example of the component modification of a resistor, a capacitor or a coil (logical circuit: original);

Fig. 20 shows an example of the component modification of a resistor, a capacitor or a coil

(transmission line circuit);

Fig. 21 shows an example of the component modification of a resistor, a capacitor or a coil (logical circuit: after modification);

Fig. 22 shows an example of component addition (logical circuit: original);

Fig. 23 shows an example of component addition (transmission line circuit);

Fig. 24 shows an example of component addition (logical circuit: after modification);

Fig. 25 shows an example of component deletion (logical circuit: original);

Fig. 26 shows an example of component deletion (transmission line circuit);

Fig. 27 shows an example of component deletion (logical circuit: after modification);

Fig. 28 shows the overall configuration of the second preferred embodiment of the present invention;

Fig. 29 shows the overall configuration of the third preferred embodiment of the present invention;

Fig. 30 shows the configuration of the logical circuit designing device; and

Fig. 31 shows the loading into a computer of a program in the present invention.

Description of the preferred Embodiments

The preferred embodiments of the present invention are described below with reference to the drawings.

To solve the problem, the present invention adopts the following configurations.

According to one aspect of the present invention, the logical circuit designing device comprises a logical circuit storage unit for storing a logical circuit, a transmission line circuit generation unit for generating a transmission line circuit based on the logical circuit stored in the logical circuit storage unit and a transmission line circuit storage unit for storing the transmission line circuit generated by the transmission line circuit generation unit.

According to another aspect of the present invention, the logical circuit designing device comprises a logical circuit storage unit for storing a logical circuit, a transmission line circuit storage unit for storing a transmission line circuit corresponding to the logical circuit stored in the logical circuit storage unit, a transmission line circuit editing unit for editing the transmission line circuit stored in the transmission line circuit storage unit and a logical circuit modification unit for

modifying the corresponding logical circuit based on the transmission line circuit edited by the transmission line circuit editing unit.

According to another aspect of the present invention, the logical circuit designing device comprises a logical circuit storage unit for storing a logical circuit, a transmission line circuit generation unit for generating a transmission line circuit based on the logical circuit stored in the logical circuit storage unit, a transmission line circuit storage unit for storing the transmission line circuit generated by the transmission line circuit generation unit, a transmission line circuit editing unit for editing the transmission line circuit stored in the transmission line circuit storage unit and a logical circuit modification unit for modifying the corresponding logical circuit based on the transmission line circuit edited by the transmission line circuit editing unit.

The logical circuit designing device of the present invention further comprises a topology designation table for storing topology information indicating the type of the connection between active components composing a logical circuit and it is preferable for the transmission line circuit generation

unit to generate a transmission line circuit based on the topology information stored in the topology designation table.

The logical circuit designing device of the present invention further comprises a value designation table for storing the value of a passive component composing a logical circuit, and it is preferable for the transmission line circuit generation unit to generate a transmission line circuit based on the value stored in the value designation table.

The logical circuit designing device of the present invention further comprises an addition designation table for storing the addition information of a passive component composing a logical circuit, and it is preferable for the transmission line circuit generation unit to generate a transmission line circuit by adding the passive component based on the passive component addition information stored in the addition designation table.

The logical circuit designing device of the present invention further comprises a deletion designation table for storing the addition information of a passive component composing a logical circuit, and it is preferable for the transmission line circuit generation unit to generate a transmission line circuit

by deleting the passive component based on the passive component deletion information stored in the deletion designation table.

In the logical circuit designing device of the present invention, it is also preferable for the logical circuit modification unit to modify the logical circuit stored in the logical circuit storage unit based on the transmission line circuit edited by the transmission line circuit editing unit.

In the logical circuit designing device of the present invention, it is also preferable for the logical circuit modification unit to modify the value of the passive components of the logical circuit stored in the logical circuit storage unit based on the transmission line circuit edited by the transmission line circuit editing unit.

In the logical circuit designing device of the present invention, it is also preferable for the logical circuit modification unit to modify the passive component addition information of the logical circuit stored in the logical circuit storage unit based on the transmission line circuit edited by the transmission line circuit editing unit.

In the logical circuit designing device of the present invention, it is also preferable for the logical

circuit modification unit to modify the passive component deletion information of the logical circuit stored in the logical circuit storage unit based on the transmission line circuit edited by the transmission line circuit editing unit.

In the logical circuit designing device of the present invention, it is also preferable for the logical circuit modification unit to modify the logical circuit based on the difference between the transmission line circuit edited by the transmission line circuit editing unit and the logical circuit stored in the logical circuit storage unit.

Fig. 1 shows the overall configuration of a logical circuit designing device adopting the present invention.

The logical circuit designing device 50 shown in Fig. 1 comprises a logical circuit storage unit 51, a transmission line circuit generation unit 52, s transmission line circuit storage unit 53, a transmission line circuit editing unit 54, a logical circuit modification unit 55 and a designation table 56.

The logical circuit storage unit 51 stores a logical circuit.

The transmission line circuit generation unit 52

generates a transmission line circuit based on the logical circuit stored in the logical circuit storage unit 51.

The transmission line circuit storage unit 53 stores the transmission line circuit generated by the transmission line circuit generation unit 52 or the transmission line circuit corresponding to the logical circuit stored in the logical circuit storage unit 51.

The transmission line circuit editing unit 54 edits the transmission line circuit stored in the transmission line circuit storage unit 53.

The logical circuit modification unit 55 modifies the corresponding logical circuit or the generated logical circuit, based on the transmission line circuit edited by the transmission line circuit editing unit 54.

The designation table 56 further comprises a topology designation table 57, a value designation table 58, an addition designation table 59 and a deletion designation table 60.

The topology designation table 57 stores topology information indicating the type of the connection between active components composing a logical circuit. Then, the transmission line circuit generation unit 52 generates a transmission line circuit based on the

topology information stored in the topology designation table 57.

The value designation table 58 stores the value of a passive component composing a circuit. Then, the transmission line circuit generation unit 52 generates a transmission line circuit based on the value stored in the value designation table 58.

The addition designation table 59 stores the addition information of a passive component composing a logical circuit. . Then, the transmission line circuit generation unit 52 generates a transmission line circuit by adding the passive component based on the passive component addition information stored in the addition designation table 59.

The deletion table 60 stores the deletion information of a passive component composing a logical circuit. Then, the transmission line circuit generation unit 52 generates a transmission line circuit by deleting the passive component based on the passive component deletion information stored in the deletion designation table 60.

The logical circuit modification unit 55 modifies the logical circuit stored in the logical circuit storage unit 51 based on the transmission line circuit edited by the transmission line circuit editing unit

54.

The logical circuit modification unit 55 also modifies the value of the passive component, passive component addition information or passive component deletion information of the logical circuit stored in the logical circuit storage unit 51.

The logical circuit modification unit 55 also modifies the logical circuit based on the difference between the transmission line circuit edited by the transmission line circuit editing unit 54 and the logical circuit stored in the logical circuit storage unit 51.

Fig. 2 shows the principle of a logical circuit designing device adopting the present invention.

The logical circuit designing device 1 comprises a logical circuit system 2 for designing a logical circuit and generating a transmission line circuit based on the logical circuit and a transmission line circuit system 3 for editing a transmission line circuit and feeding back (reflecting) the editing result to (on) the logical circuit, that is, modifying the logical circuit.

The logical circuit system 2 comprises a logical circuit database (DB) 21 for storing a logical circuit, a topology designation table 22 for storing topology

information indicating the type of the connection between active components composing a logical circuit, a value designation table 23 for storing the values of passive components composing a circuit, an addition designation table 24 for storing the addition information of passive components composing a logical circuit and a deletion designation table 25 for storing the deletion information of passive components composing a logical circuit.

The logical circuit system 2 extracts a logical circuit from the logical circuit DB 21 and generates a transmission line circuit DB 31.

The logical circuit system 2 also extracts a logical circuit from the logical circuit DB 21 and generates a transmission line circuit DB 31 with the value of a passive component, such as a resistor, a capacitor, a coil and the like, set to the value specified in the value designation table 23.

The logical circuit system 2 also extracts a logical circuit from the logical circuit DB 21 and generates a transmission line circuit DB 31 with a passive component, such as a resistor, a capacitor, a coil and the like, specified in the addition designation table 24 added.

The logical circuit system 2 also extracts a

logical circuit from the logical circuit DB 21 and generates a transmission line circuit DB 31 with a passive component, such as a resistor, a capacitor, a coil and the like, specified in the addition designation table 24 deleted.

The transmission line circuit system 3 also comprises a transmission line circuit DB 31 for storing a transmission line circuit corresponding to the logical circuit.

The transmission line circuit system 3 inputs both the logical circuit DB 21 and transmission line circuit DB 31 of the logical circuit system 2, extracts the value modification information of a passive component, such as a resistor, a capacitor, a coil and the like, from the difference between the logical circuit DB 21 and transmission line circuit DB 31 and modifies the logical circuit DB 21 based on this values.

The transmission line circuit system 3 also inputs both the logical circuit DB 21 and transmission line circuit DB 31 of the logical circuit system 2, extracts the modification information of each passive component from this difference and modifies the logical circuit DB 21 based on this modification information.

The transmission line circuit system 3 also inputs both the logical circuit DB 21 and transmission line

circuit DB 31 of the logical circuit system 2, extracts the addition information of each passive component from this difference and modifies the logical circuit DB 21 based on this addition information.

The transmission line circuit system 3 also inputs both the logical circuit DB 21 and transmission line circuit DB 31 of the logical circuit system 2, extracts the deletion information of each passive component from this difference and modifies the logical circuit DB 21 based on this deletion information.

Next, the first preferred embodiment of the present invention is described with reference to Figs. 3 through 27.

Fig. 3 shows the overall configuration of the first preferred embodiment of the present invention.

A transmission line circuit DB generation unit 20 generates a transmission line circuit DB 31 based on both the logical circuit DB 21 and designation data stored in the designation table 56 (at least one of topology designation table 22, value designation table 23, addition designation table 24 and deletion designation table 25).

A logical circuit DB generation unit 30 regenerates (modifies) the logical circuit DB 21 by extracting the difference between a modification

(editing) content in the transmission line circuit system 3 and the original logical circuit DB 21.

Fig. 4 shows an example of topology designation (general).

In Fig. 4, a driver A is connected to receivers X, Y and Z.

Fig. 5 shows an example of topology designation (star type).

In Fig. 5, a driver A is connected to receivers X, Y and Z in a shape of a star. Therefore, the designation of such a connection is called star type.

Fig. 6 shows an example of topology designation (one-stroke brushing type).

In Fig. 6, a driver A is connected to a receiver X, then the receiver X is connected to a receiver Y and the receiver Y is further connected to a receiver Z. Therefore, the designation of such a connection is called one-stroke brushing type.

Next, the value designation of a passive component (resistor, capacitor, coil, etc.) is described with reference to Figs. 7 through 9.

Fig. 7 shows an example of the value designation of a resistor, a capacitor or a coil (logical circuit).

In Fig. 7, the value of a resistor R1 provided between a driver A and receivers X and Y is 20Ω in a

logical circuit.

Fig. 8 shows an example of the value designation of a resistor, a capacitor or a coil (value designation table).

Fig. 8 shows the structure of the value designation table 23 in the case where the value of a resistor R1 is designated as 33Ω.

Fig. 9 shows an example of the value designation of a resistor, a capacitor or a coil (transmission line circuit).

In Fig. 9, the value of a resistor R1 provided between a driver A and receivers X and Y is designated as 33Ω in a transmission line circuit diagram by value designation.

Next, the addition designation of a passive component (resistor, capacitor, coil, etc.) themselves is described with reference to Figs. 10 through 12.

Fig. 10 shows an example of the addition designation of a resistor, capacitor or coil (logical circuit).

In Fig. 10, a driver A is connected to receivers X and Y by a NET 1 (a driver A and receivers X and Y constitute a network).

Fig. 11 shows an example of the addition designation of a resistor, a capacitor or a coil

(addition designation table).

Fig. 11 shows the structure of the addition designation table 24 in the case where a 33Ω resistor is added by the side of a driver A in a network (NET1) composed of the driver A and receivers X and Y.

Fig. 12 shows an example of the addition designation of a resistor, a capacitor or a coil (transmission line circuit).

In Fig. 12, a 33Ω resistor is provided by the side of a driver A in a network (NET1) consisting of the driver A and receivers X and Y by passive component (resistor) addition.

Next, the deletion designation of a passive component (resistor, capacitor, coil, etc.) is described with reference to Figs. 13 through 15.

Fig. 13 shows an example of the deletion designation of a resistor, capacitor or coil (logical circuit).

In Fig. 13, a 100Ω resistor R1 is provided between a driver A and receivers X and Y in a logical circuit.

Fig. 14 shows an example of the deletion designation of a resistor, capacitor or coil (addition designation table).

Fig. 14 shows the structure of the deletion designation table 25 in the case where a resistor R1

is deleted.

Fig. 15 shows an example of the deletion designation of a resistor, capacitor or coil (transmission line circuit).

In Fig. 15, a 100Ω resistor R1 provided between a driver A and receivers X and Y, is deleted by passive component (resistor) deletion.

Next, the value modification of a passive component (resistor, capacitor, coil, etc.) is described with reference Figs. 16 through 18.

Fig. 16 shows an example of the value modification of a resistor, capacitor or coil (logical circuit: original).

In Fig. 16, the value of a resistor R1 provided a driver A and receivers X and Y is 20Ω in a logical circuit.

Fig. 17 shows an example of the value modification of a resistor, capacitor or coil (transmission line circuit).

In Fig. 17, the value of the resistor R1 is modified from 20Ω to 33 Ω in a transmission line circuit.

Fig. 18 shows an example of the value modification of a resistor, capacitor or coil (logical circuit: after modification).

In Fig. 18, the value of the resistor R1 provided

between the driver A and receivers X and Y is already modified to 33Ω by value modification.

Next, the component modification of a passive component (resistor, capacitor, coil, etc.) is described with reference to Figs. 19 through 21.

Fig. 19 shows an example of the component modification of a resistor, capacitor or coil (logical circuit: original).

In Fig. 19, the value in a logical circuit of a capacitor C1 provided between a driver A and receivers X and Y, is 1μF.

Fig. 20 shows an example of the component modification of a resistor, capacitor or coil (transmission line circuit).

In Fig. 20, the capacitor C1 is modified to a 33Ω resistor R1 in a transmission line circuit.

Fig. 21 shows an example of the component modification of a resistor, capacitor or coil (logical circuit: after modification).

In Fig. 21, the 1μF capacitor C1 provided between the driver A and receivers X and Y, is already modified to the 33Ω resistor R1.

Next, the modification of an active component (driver, receiver, etc.) is described with reference to Figs. 22 through 24.

Fig. 22 shows an example of component addition (logical circuit).

In Fig. 22, a 33Ω resistor R1 is provided between a driver A and receivers X and Y in a logical circuit.

Fig. 23 shows an example of component addition (transmission line circuit).

In Fig. 23, a receiver Z is added to the receiver X and Y side.

Fig. 24 shows an example of component addition (logical circuit: after modification).

In Fig. 24, the 33Ω resistor R1 is now provided between the driver A and receivers X, Y and Z, that is, the receiver Z is newly added.

Next, the deletion of an active component (driver, receiver, etc.) is described with reference to Figs. 25 through 27.

Fig. 25 shows an example of component deletion (logical circuit: original)..

In Fig. 25, a 33Ω resistor R1 is provided between a driver A and receivers X, Y and Z in a logical circuit.

Fig. 26 shows an example of component deletion (transmission line circuit).

In Fig. 26, the receiver Y on the receiver X, Y and Z side is deleted.

Fig. 27 shows an example of component deletion

(logical circuit: after modification).

In Fig. 27, the 33Ω resistor R1 is now provided between the driver A and receivers X and Z, that is, the receiver Y is now deleted.

Next, the second preferred embodiment of the present invention is described.

Fig. 28 shows the overall configuration of the second preferred embodiment of the present invention.

The transmission line circuit DB generation unit 20 generates a transmission line circuit DB 31 based on both the logical circuit DB 21 and designation data stored in the designation table 56 (at least one of topology designation table 22, value designation table 23, addition designation table 24 and deletion designation table 25).

Next, the third preferred embodiment of the present invention is described.

Fig. 29 shows the overall configuration of the third preferred embodiment of the present invention.

The logical circuit DB generation unit 30 regenerates (modifies) the logical circuit DB 21 by extracting the difference between a modification (editing) content in the transmission line circuit system 3 and the original logical circuit DB 21.

Although the preferred embodiments of the present

invention have been described above with reference to the drawings, the logical circuit CAD apparatus adopting the present invention is not limited to the preferred embodiments described above only if the function can be executed. The apparatus can be a single apparatus, a system consisting of a plurality of apparatuses or integrated apparatus, or a system for performing the process through a network, such as a LAN, WAN and the like.

As shown in Fig. 30, the logical circuit CAD apparatus can also be implemented by a system comprising a CPU 141, a memory 142, such as a ROM and a RAM, an input device 143, an output device 144, an external storage device 145, a medium driving device 147, a portable storage medium 146, a network connection device 148, which are all connected to a bus 140. Specifically, the function of the preferred embodiment described above can also be implemented by providing the logical circuit CAD apparatus with the memory 142, such as a ROM and a RAM, external storage device 145 or portable storage medium 146 which store the program codes software program codes for implementing the system in the preferred embodiment described above and by enabling the computer of the logical circuit CAD apparatus to read and execute the program codes.

In this case, the program codes read from the portable storage medium 146 and the like enable the computer to implement the new function of the present invention, and the portable storage medium 146 and the like which stores the program codes constitutes the present invention.

For the portable storage media for providing the program codes, for example, a flexible disk, a hard disk, an optical disk, a magneto-optical disk, a CD-ROM, a CD-R, a DVD-ROM, a DVD-RAM, a magnetic tape, a non-volatile memory card, a ROM card, a variety of storage media that store the program codes through the network connection device (in other words, communications line), such as an electronic mail, personal communications, etc., and the like can be used.

Although the function of the preferred embodiment described above can be implemented by enabling a computer 150 to execute the program codes read in a memory 151, as shown in Fig. 31, the function can also be implemented by enabling an OS that is operated in the computer and the like to perform a part or all of the actual process according to the instructions of the program codes.

Furthermore, the function of the preferred embodiment described above can also be implemented by

writing the program codes read from the portable storage medium 152 and program/data 153 provided by a program/data provider in the memory 151 which is provided in a function extension board inserted in the computer 150 or provided in a function extension unit connected to the computer 150 and then enabling a CPU and the like which is provided in the function extension board or unit to perform a part or all of the actual process.

In other words, the present invention is not limited to the preferred embodiments described above and can take a variety of configurations or structures within the scope of the objective of the present invention.

As described above, according to the present invention, work that has manually been done can be automated. Therefore, labor can be reduced and data reliability can be improved.